

Remarks

In the Office Action dated July 26, 2010, the following rejections are maintained: claims 17-19 stand rejected under 35 U.S.C. § 112(1); claims 1, 3, 5, 7 and 17-19 stand rejected under 35 U.S.C. § 103(a) over Chang (U.S. Patent No. 5,991,204) in view of Sharma (U.S. Patent 5,488,579) and further in view of a Quirk reference (“Semiconductor Manufacturing Technology”); claims 4 and 14 stand rejected under 35 U.S.C. § 103(a) over the ‘204, ‘579 and Quirk references and further in view of Hong (U.S. Patent No. 5,614,746); and claim 6 stands rejected under 35 U.S.C. § 103(a) over the ‘204, ‘579 and Quirk references and further in view of Chen (U.S. Patent No. 6,091,104). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Advisory Action dated June 10, 2009, or the Office Actions of record.

Applicant renews the traversal of the Office Action’s assertion that the limitation “using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer” is a functional limitation. As previously asserted by Applicant, the label of “functional limitation” is inapplicable to a step within a method claim. As M.P.E.P § 2114 illustrates, the law regarding the functional limitations is directed at the use of language attempting to describe the features of an apparatus based on the functions they perform in an apparatus claim. As the claims currently under examination are method claims, any distinction of particular limitations based on an assertion of the limitation as a functional limitation or includes functional language is improper. In presenting a *prima facie* case of obviousness the Examiner is under an obligation to assert correspondence to all of the claim limitations, including those directed to “using the spacers to mitigate the diffusion of oxygen.”

Applicant traverses the § 103(a) rejections because the Office Action fails to present a *prima facie* case of obviousness. In presenting a *prima facie* case of obviousness, the Examiner must consider “both the invention and the prior art references as a whole.” M.P.E.P. §2141.02. Further, the Examiner is reminded that “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since

uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-419 (U.S. 2007). The rejections presented in the Office Action appear to attempt to combine the spacers of the secondary ‘579 reference with the gate stack of the flash EEPROM device of the primary ‘204 reference without regards to overall teachings of either the primary ‘204 reference or the secondary ‘579 reference. The present rejection amounts to the assertion that simply finding a spacer made of a material that has an oxygen diffusion an order of magnitude smaller than the oxygen diffusion through the oxide spacer results in the combination being obvious. Allowing such a rejection to stand strips the rejection of any necessary motivation to combine and results in a rejection based on finding the various limitations scattered throughout various references regardless of the actual teachings of the cited references. This is contrary to the M.P.E.P. and relevant case law, including *KSR*.

The § 103(a) rejections are further improper because the cited combination of references lacks correspondence. For example, none of the asserted references teaches the claimed invention “as a whole” (§ 103(a)) including aspects regarding forming a control gate and a floating gate separated by an interlayer dielectric layer, with spacers that are both arranged and used to mitigate oxygen diffusion to the interlayer dielectric layer. Because none of the references teach these aspects, no reasonable combination of these references can provide correspondence. As such, the § 103 rejections fail.

The asserted spacers in the secondary ‘579 reference do not and cannot mitigate oxygen diffusion as suggested because their arrangement in the ‘579 reference as part of an inverted gate structure does not permit the spacers to do so. Combining the inverted-gate manufacturing approach of the ‘579 reference with the (conventional) gate stack of the flash EEPROM device in the primary ‘204 reference does not result in the claimed method as suggested in the Office Action. Essentially, the Examiner’s rejection relies upon an assertion that *if* the spacers of the ‘579 reference were arranged in an as yet undisclosed manner to mitigate oxygen diffusion, *then* the cited spacers *could* mitigate oxygen diffusion to an interlayer dielectric material; however, nothing in the record establishes that the purported combination of an inverted-gate structure with the gate stack in the ‘204 reference would correspond, and nothing in the record suggests doing so

in order to mitigate diffusion (in the context of the method-based limitations or otherwise).

The cited spacers in the inverted gate structure of the ‘579 reference cannot and do not mitigate oxygen diffusion as claimed because they are not positioned to do so. The inverted gate structure in the ‘579 reference is further unrelated to the (conventional) structure of the ‘204 reference and issues relating to the manufacture of the same. Due to this inverted structure, gate oxides 35 and 38 of the ‘579 reference are completely exposed during any subsequent oxide growth, relative to the spacers 37. The cited spacers 37 therefore do not mitigate the diffusion of oxygen in an interlayer dielectric layer because such layers are formed over the spacer (e.g., tunnel oxide 38 is formed over and after the spacer 37, which thus cannot mitigate any diffusion as asserted). The Office Action is further silent as to how to combine the inverted-gate manufacturing approach of the ‘579 reference with the manufacture of a conventional gate stack for the EEPROM device in the ‘204 reference. Accordingly, none of the cited references teach or suggest limitations directed to using spacers to both mask an underlying gate and mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

The Examiner’s arguments on pages 13-14 of the Office Action dated July 26, 2010, further illustrate the Examiner’s misapplication of the law. Specifically, the Examiner ignores the specific teachings of the secondary ‘579 reference regarding the location of the asserted spacers, and argues that “the oxygen has to diffuse across the spacer before reaching the interlayer dielectric layer.” However, as previously asserted by Applicant, and as illustrated in Figure 4, for example, of the ‘579 reference, the asserted spacers 37 are covered by the oxide layer 38, and as such oxygen cannot diffuse across the spacer to reach the dielectric layer, but rather would diffuse through the dielectric layer to reach the spacer. The Office Action’s arguments continue to ignore the teachings of the ‘579 reference regarding the location of the asserted spacers. Accordingly the § 103(a) rejections are improper and should be withdrawn.

The §103(a) rejections are further improper because Office Action fails to provide proper motivation to combine the cited inverted-gate manufacturing approach of the ‘579 reference with the gate stack manufacturing steps of the ‘204 reference. Specifically, the Examiner has failed to provide any explanation as to how the inverted-gate

manufacturing approach in the ‘579 reference, which uses a nitride spacer 37 to “smooth the topography created by the polysilicon gate 36” and to address specific problems with inverted-gate structures as in FIG. 3, would apply to the conventional gate stack of the EEPROM device in the ‘204 reference. Nothing in the asserted art either explains how this inverted-gate approach would either be applicable to or combined with the EEPROM gate stack in the ‘204 reference. Further, the asserted embodiment of the ‘204 reference does not appear to include layers overlying the asserted control gate. Accordingly, one of skill in the art would not be motivated to use the asserted spacers in order to eliminate sharp corners or edges to prevent protrusion into the nonexistent overlying layers.

Moreover, Applicant fails to recognize how this combination of teachings would result in an implementation that is operable and consistent with the objectives of the ‘204 reference. As consistent with the M.P.E.P. and relevant case law, if a “proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.” *See* M.P.E.P. 2143.01, citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). This attempt at modifying the ‘204 reference without providing examples from the prior art in support of such modification is further contrary to § 103 and relevant law (*see KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007), requiring evidence of motivation where the primary reference is modified).

The Office Action has also failed to establish motivation to combine the dry etch of the Quirk reference with the ‘204 reference, as consistent with Applicant’s traversals of record, contrary to the requirements of the M.P.E.P. and applicable law (*see, e.g.*, the *KSR* reference as cited above). In this instance, the alleged motivation to combine the Quirk reference with the ‘204 reference is to provide “high selectivity and low device damage” but is silent as to how these features would be applicable to the conventional gate structure of the ‘204 reference or how the ‘204 reference could function as such. For example, while the Office Action provides no discussion as to how the dry etch in the Quirk reference would be combined with the ‘204 reference as modified with the inverted-gate approach as shown in the ‘579 reference, it appears such a dry etch would be inapplicable as there are no underlying dielectric regions due to the inverted nature of the structure.

Applicant traverses the § 112(1) rejection of claims 17-19 for failure to comply with the written description requirement. Support for the limitation at issue can be found on page 4, lines 18-21. Specifically, in the alternative embodiment mentioned on page 4 and referenced at page 9, line 16, the interlayer dielectric layer is present under the spacers 81. Accordingly, a portion of the interlayer dielectric layer is masked. Applicant therefore requests the § 112(1) rejection of claims 17-19 for failure to comply with the written description requirement be withdrawn.

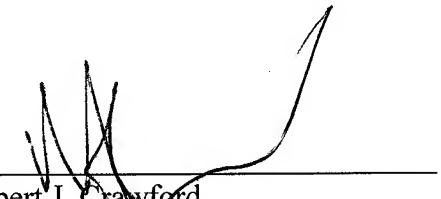
Applicant further traverse the § 112(2) rejection of claims 17-19. One of skill in the art reading the claim would understand that “the tunnel dielectric layer” refers to the previously recited “tunnel dielectric”. Accordingly, the lack of proper antecedent basis rises, at most, to the level of an objection. Notwithstanding, and in an effort to facilitate prosecution, Applicant has amended claim 17. Therefore, Applicant respectfully requests the amendment be entered and the rejection be withdrawn.

Applicant maintains its traversals regarding the restriction requirement for reasons as stated in the record, as the rationale provided in support of the restriction is misguided and fails to comply with the requirements of the M.P.E.P., that the Examiner establish that a serious burden exists. Specifically, M.P.E.P. § 803 indicates that establishing a *prima facie* serious burden can be shown “by appropriate explanation of separate classification, or separate status in the art, or a different field of search as defined in MPEP § 808.02.” In this instance, the Office Action fails to establish such *prima facie* burden in attempting to support the restriction by asserting that “there were a lot of amendments.” The Examiner’s assertion that examining these claims as amended would present “undue burden” fails to meet the *prima facie* requirements as discussed in the M.P.E.P. Further, the Examiner’s response stating that “the examiner really found undue burden during the execution” fails to provide the support needed to establish that such a burden existed. Simply stating that something is so does not make it true. The Examiner must provide some factual basis or “appropriate explanation” of the burden asserted. Applicant therefore submits that the restriction is improper, and further believes that the claims should be allowable over the cited references for reasons including those stated in the record and herein.

In view of the above, the § 103 rejections are improper and Applicant requests that they be withdrawn. Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilska, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

By: 
Robert J. Crawford
Reg. No.: 32,122
(NXPS.442PA)

CUSTOMER NO. 65913